QFO-AP-FI-MO02	Course Syllabus :اسم النموذج	جامعة فيلادلفيا Philadelphia University
رقم الاصدار : 1 (Revision)	الجهة المصدرة: كلية تكنولوجيا المعلومات	
التاريخ :2017/11/05	الجهة المدققة: عمادة التطوير والجودة	
عدد صفحات النموذج:		

Course Title: Computer Architecture	**Course code: 750332**
Course Level: 3	**Course prerequisite (s): 750233+731110**
Lecture Time:	**Credit hours: 3**

Academic Staff Specifics

Name	Rank	Office Number and Location	Office Hours	E-mail Address

Course module description:

The module emphasizes on the following knowledge areas: Digital components used in the organization and design of digital computer, serial and parallel transfer, Flow of information and timing signals. Designing a micro-programmed control unit, organization and architecture of input-output and memory, interfacing and communication, memory hierarchy, cache memory, Virtual Memory, pipelining data path, pipelining control path, and data hazard.

Course module objectives:

The aim of this course is to introduce organization and architecture of the computer components.

Course/ module components:

- **Basic Computer Organization.**
- **Control unit and Control memory.**
- **Micro-instruction.**
- **Input-Output Organization.**
- **Memory Organization.**
- **Cache Memory.**
- **Virtual Memory**
- **Pipelining data path and Control path.**
- **Data Hazard.**

Text Book:

Book(s): Computer System Architecture, M. Morris Mano, Prentice Hall, International edition, 2005. 4rd edition.

Learning outcomes:

A. Knowledge and understanding

A1. List and explain the various instructions formats and instruction type.
A2. Explain the concept of CPU instruction set architecture (ISA).
A3. Know the design and implementation of a control unit made of micro-programming.

B. Intellectual Skills

B1. Know the design and implementation of a control unit made of micro-programming.
B2. Know how memory organization can improve the overall computer performance.
B3. Know how memory organization can improve the overall computer performance.

C. Practical Skills

C1. Know the basic structure of a typical RISC and CISC processor.
C2. Know the effect of pipelining on the CPU performance in comparing with single cycle instruction CPU.
C3. Be able to prepare computer specifications.

D. Transferable Skills

D1. Understand how memory hierarchy and pipelining affects the performance of a processor.
D2. Understand the communication (input/output) issues.
D3. Know some computers design.

Learning outcomes achievement

Development:

A1, A2, and A3 are developed through the lectures.

B1, C3, and D3 are developed through Tutorials.

D1, D2, B3 are developed through Homework.

Assessment: A2, B2, D1 are assessed through Quizzes, written Exams.

B3, D2, C2, and A3 are assessed through home work exam.

Assessment instruments:

Allocation of Marks	
Assessment Instruments	**Mark**
First examination.	**20**
Second examination.	**20**
Final examination.	**40**
Quizzes, Home works.	**20**
Total	**100**

** Make-up exams will be offered for valid reasons only with consent of the Dean. Make-up exams may be different from regular exams in content and format.*

Practical Submissions:

The assignments that have work to be assessed will be given to the students in separate documents including the due date and appropriate reading material.

Course/module academic calendar

Week	Basic and support material to be covered
(1 and 2)	**Review of Basic Computer Organization** - Register Transfers. - Bus and Memory Transfers. - Computer Instruction. - Memory Organization.
(3 ,4 and 5)	**Micro-programmed Control Unit** - Control Memory. - Address Sequencing and Control Branching. - Mapping of instruction. - Design of Control Unit using Micro-programming..
(6, 7 and 8) **First Exam**	**Input-Output Organization** - Peripheral Devices. - Input-output Bus and Interface Modules. - Input-output Bus Versus Memory Bus. - Priority Interrupt: Daisy-Chaining and Parallel interrupt. - Direct Memory Access (DMA). .

(9, 10 and 11) **Second Exam**	**Memory Organization** - Memory Hierarchy. - Main Memory: RAM and ROM Chips. - Memory Address Map. - Cache Memory. - Virtual Memory.
(12, 13, and 14)	**Pipelining and Vector Processing** - Parallel Processing. - Pipelining. - Instruction Pipeline. - Pipeline data path and Control path. - Data Hazard.
(15)	**RISC and CISC Architecture** - Characteristics of RISC and CISC.
(16) **Final Exam**	**Review**

Expected workload:

On average students need to spend 2 hours of study and preparation for each 50-minute lecture/tutorial.

Attendance policy:

Absence from lectures and/or tutorials shall not exceed 15%. Students who exceed the 15% limit without a medical or emergency excuse acceptable to and approved by the Dean of the relevant college/faculty shall not be allowed to take the final examination and shall receive a mark of zero for the course. If the excuse is approved by the Dean, the student shall be considered to have withdrawn from the course.

Module references:

a) Books:

1. The Architecture of Computer Hardware and System Software, Irv Englander, John Wiley and Sons**,** 2005, 3nd edition.
2. Fundamentals Of Computer Organization And Architecture**.** Mostafa Abd-El-Barr, Hesham El-Rewini. John Wiley and Sons**,** 2008, 3nd edition.

b) Journals:

Article title COMPUTER ARCHITECTURE AND ORGANIZATION IN THE MODEL COMPUTER ENGINEERING CURRICULUM

Author Nelson, V. P. Theys, M. D. Clements, A.

Journal title FRONTIERS IN EDUCATION CONFERENCE

Bibliographic details 2003, VOL 2, pages F2F-11-F2F-16

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Websites:

1) http://williamstallings.com/COA6e.html

2) http://www.ece.eng.wayne.edu/~gchen/ece4680/lecture-notes/lecture-notes.html