Abstracts

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Paper 1

"Stroboscopic Measurements of Strip Domain Expansion in Chevron Stacks". Joint 3M / Intermag. Conf., New York, and J. App. Physics. Vol. 50, p. 7871 (abs) (1979).

Abstract: Domain motion and stretching in bubble device chevron expander stacks is characterized over the frequency range 100 kHz to 500 kHz. Lateral motion through the stacks shows stable resting positions at the two ends and at the center of the chevrons with the strip transferring quickly between these positions. The transfer requires a progressively longer phase angle as the frequency is increased, and this reduces the resting phases correspondingly, e.g. at the apex from 45˚ at 100 kHz to 10˚ at 500 kHz. Transverse expansion takes place principally during the pauses at the ends of the chevrons. The form of the stretching is largely linear with phase, but slows to a limiting value before a lateral transition occurs. However, the linear region reduces in phase-width at increased frequencies to allow only minimal expansion, combined with a small contraction when crossing the gap between stacks, at frequencies above 400 kHz. Some asymmetry in the stretching is noted, related to different velocity variations with bias in the two directions.

paper 2

"Vacuum Deposition and Evaluation of Constituent Layers of Cu2S/CdS Solar Cell". Journal of Solar Energy Research Baghdad, Vol. 4, No.2, P. 82, Sep. (1986).

Abstract: The layers constituting Cu_2S/CdS solar cell have been vacuum deposited and examined individually. It is found that in order to fabricate stable films of $CdSCu_2S$ and aluminum free of cracks and pinholes and having low resistivity, the substrate temperature and vacuum pressure must be specified precisely. The resistivity of the films is found to depend on the above parameters as well as film thickness. A technique involving heat treatment and washing of the cell has been introduced to improve cell efficiency. Effect of temperature and illumination level on I-V characteristic of the improved cell has been examined.

Paper 3

"Electrical Characteristics of a $Si_{1-x}Ge_x$ Alloy Thin Films". Al-Rafidian Eng., Vol.3, No.2, Mosul University, Mosul, Iraq, P.1, (1995).

Abstract: Four samples of silicon germanium thin films deposited on a glass substrates of different percentage of germanium were fabricated. It was found that the increase in germanium percentage from 0 to 25% leads to a reduction of optical energy gap from 1.55 eV to 1.35 eV. The above samples have been deposited on silicon wafers and the photo-electrical properties of the junctions were studied. The behavior of 25% germanium sample gave, somewhat, better detection parameters (detectivity of 2000 W^{-1}) with low values of leakage current. While the 10% germanium sample gave low values of quantum efficiency because of the high value of leakage current.

Paper 4

"Study of Aluminum Thin Film Properties under Different Thermal Vacuum Deposition Parameters". Al- Rafidian Eng. Vol.3, No.2, Mosul University, Mosul, Iraq, P.38, (1995).

Abstract: Layers of aluminum thin films of thickness up to 3um have been fabricated under different thermal vacuum deposition parameters.

The rate of deposition varies linearly with the rate of evaporation when the source placed at the centre of the vacuum chamber with 10 cm distance between them. But as the substrate moved away from the renter of the chamber the rate of deposition becomes less dependence on the rate of evaporation. Also the of deposition at the centre of the chamber decreases as the pressure increases or the distance between the source and substrate increases, and this dependence fall rapidly as the substrate moves away from the centre. The relation between the rate of deposition and the distance when the substrate moved on the wall of the chamber was sinusoidal and its maximum at O=45˚, while this relation is exponential when the substrate moved at the same level of the source at high pressure and becomes nearly linear at low pressure.

Paper 5

"The Effect of Temperatures and Doped Level on CdS Thin Films". Eng. & Tech. J., Vol.14, No.7, P.34, July, (1995).

Abstract: Few of pure CdS and In-doped CdS thin films of different thicknesses were prepared using the thermal vacuum evaporation technique. The electrical characteristics of these filme were studied. It was found that the conductivity increased as the thicknesses increased up to 20000˚A. A maximum conductivity was obtained at substrate temperature around 180˚C. The conductivity is almost temperature independent for thick films (thicker than 14000˚A), while it is decreased as the temperature decreased for thinner films. Also the conductivity of the heat treated films is about two orders of magnitude greater than that of the corresponding untreated films. The conductivity is increased as the indium level is increased in CdS films. A change in activation energy is noticed due to changing the temperature. Higher activation energy is obtained at higher temperatures.

paper 6

"The Effect of Evaporation Parameters on the Deposition Rate of Metals Deposited Under Low Pressures". Al-Rafidian Sciences J., Mosul University, Mosul, Vol.7, No.1, (1996).

Abstract: Few thin films of copper, silver and aluminum have been fabricated using thermal vacuum evaporation techniques. The effect of; substrate position, angle of vapour incidence, pressure and atomic weight of the metal on the rate of deposition have been studied. It is found that the deposition rate of copper material is decreased when the substrate moved away from the center of vacuum chamber. This result was also true when the substrate was placed either at the top or bottom of the chamber. Pressure effect was more pronounced on the rate of deposition when the substrate was at the same level of the source. The deposition rare of the same material was increased when the substrate placed at the wall of the chamber and moved up. The maximum deposition rate was obtained at (30˚) angle of incidence. The effect of atomic weight on the rare of deposition has been studied. Two different results are obtained. The first one that the deposition rate is increased when the atomic weight is increased for the substrate placed at the top or the wall of the chamber. Second the deposition rate is decreased when the atomic weight is increased for the substrate placed close and at

the same level of the source. The effect of atomic weight becomes negligible when the substrate moved away form the source.

Paper 7

"Some Aspects of Alloying and Crystallization of Amorphous Silicon Germanium Thin Films". Mu'tah Lil-Buhuth Wad-Dirasat Vol. 12, No. 3, P.63 (April 1997).

Abstract: A series of a-$Si_{1-x}Ge_x$ thin films have been deposited on two types of substrates, micro glass and silicon wafer, using vacuum thermal evaporation technique. The effects of annealing temperature and germanium quantity on the structural and electrical properties of the prepared films have been studied, while the rest of deposition parameters (thickness, deposition rate, vacuum pressure and substrate temperature) are fixed throughout the tests. Using x-ray spectrometer, it was found that there is a difference in the germanium quantity between the calculated values of the prepared alloys before evaporation and the values of the germanium in the deposited films. The results obtained using x-ray diffraction technique showed that all fabricated samples were amorphous at the beginning. The polycrystalline structure is initiated at annealing temperature equal to 600˚C for the samples deposited on glass substrate, but the crystalline structure is distorted above this temperature. While the crystalline structure of the samples fabricated on Si-wafer becomes more pronounced at higher annealing temperature. Surface I-V characteristics share the proves that higher annealing temperature and germanium quantity shows higher degree of crystallization and higher forward current and small reverse current through the Heterojunction.

Paper 8

"The Electrical Properties of Thermal Vacuum Deposition CdS Thin Films" Eng. & Tech. J., University of Technology, Vol.17, No.12, P.1114, (1998).

Abstract: This research is intended as a study of electrical properties of CdS thin films fabricated by vacuum thermal evaporation technique. The CdS films characteristics have been studied as a function of different fabrication conditions such as: thickness, deposition temperature, annealing temperature, and deposition rate. The best of these conditions were: 12000˚A thickness, 180˚C deposition temperature, 250˚C annealing temperature and 2˚A/sec as a rate of deposition. I-V characteristics shows that the current is directly related to the biasing voltage, film thickness and annealing temperature up to 250˚C, and inversely related to the deposition rare. The contacts to the films were thin films of aluminum metal, these were ohmic contacts. The fabricated films were found to be n-type and after applying the optimized fabrication conditions, it is found that the maximum values of carrier concentration and Hall mobility are: 5×10^{16} cm^{-3} and 9.7 cm/V.sec respectively.

Paper 9

"The Photo-Electric and Thermal Properties of Vacuum Deposited CdS Thin Films". Renewable Energy Journal Vol. 14(1-4), (May-August 1998).

Abstract: This research is intended to study the photo-electric and thermal characteristics of CdS thin films. These films were fabricated using vacuum thermal evaporation techniques. The prepared samples were found to have a good light response. It is observed that the photocurrent is linearly proportional to the film thickness, substrate temperature and annealing temperature up to 250 ^{o}C where at this temperature maximum photocurrent (40 □A) was obtained. Also, the photocurrent is inversely proportional to the deposition rate. 12000A film thickness

has been chosen because it has the minimum resistivity which gives the best photo-electric and thermal response. Two values of activation energy, lying between (0.064-0.28) eV for temperature range (293-473) K for different deposition parameters were obtained. Also, it was found that this energy decreased as annealing temperature increased up to 250 ^{o}C indicating that the carrier concentration increases with annealing temperature.

Paper 10

"Electro-Thermal properties of Thermal Deposited CdS Thin Films". Dirasat Journal, Jordan, Vol. 25(3), Oct. (1998).

Abstract: The electro-thermal properties of pure and doped CdS thin films fabricated by vacuum thermal evaporation are studied in this paper. Eighteen samples of different thicknesses have been fabricated at a vacuum with a pressure as less as 10^{-6} torr under different deposition parameters (Viz. Substrate temperature, deposition rate, doping level and annealing temperature). It was found that the samples have minimum resistivity at 12000˚A thickness, and the resistivity decreases as the working temperature increases. While the activation energies of the samples decreased, the sample thickness increased.

The variation of sample resistance as a function of temperature is measured by connecting the samples in series with a constant current source. The thickness of the samples was kept constant at 2000˚A, while substrate temperature, deposition rate, annealing temperature and doping level were varied. It was found that high variation of resistance with temperature is obtained at low substrate temperature, low doping level, low annealing temperature and high deposition rate.

Paper 11

"The Effect of The Series Resistance on The Photovoltaic Properties of In-doped CdTe (p) Thin Film Homojunction", Renewable Energy J., England, Vol. 21(2), P. 141, (2000).

Abstract: The photovoltaic properties of In-doped CdTe (p) thin film homojunction structure have been investigated, specially the effect of the series resistance on the short-circuit current at low and high light intensities has been discussed in detail. A simulation of the fabricated device is achieved successfully using the PSPICE computer program. Mathematical derivations are implemented in order to interpret the results. It is found that the deteriorative effect of the series resistance on the short circuit current versus light intensity characteristics increases with increasing the light intensity. A new factor has been suggested to measure how the series resistance affects the solar cell behavior at low and high light intensities.

Paper 12

"Design of Programmable Electronic System to Calculate and supervise Feeders on and off Time in Substations", Al-Rafidain Engineering, Mosul, Vol. 8(3), P. 1, (2000).

Abstract: In order to distribute the electricity power between the customers and due to the Inexistence of control and supervisory centers anew-electronic circuit has been designed. The circuit supervises and monitors the time and state of the feeders and store the information on EEPROM. Also interface circuit has been designed to read .this information by central computer. All the software needed to arrange the data has been written and applied on the computer.

Paper 13

"Infrared Response and Quantum Efficiency of In-doped Silicon (n) Structure" Renewable Energy Journal, England, Vol. 21(3-4), P. 323, Nov.-Dec. (2000).

Abstract: In order to improve and extend the sub-band gab response in n-type layer of silicon Indium should be added. In fact indium acts as an electrical dopant responsible of changing the surface layer of n-type wafer to a p-type as well as the optical dopant (IPV effect). In this research theoretical and practical calculations of short circuit currents of Indium silicon (n) structure have been calculated. Theoretically modified Shockley-Read Hall model is used to calculate the recombination rate via an impurity level. It was concluded that either the current generation decreases when the recombination rate is positive or to increase the current generation when the recombination rate is negative. The current generation equation was solved numerically using mat lab program. The maximum values of generated current was 5.25 mA at $0.5x10^{17}$ cm^{-3} indium concentration few samples of indium doped silicon (n) structure were prepared using vacuum Thermal evaporation. A thin layer of indium was deposited on the top of an n-type single crystal silicon wafer. In order to form a pn junction the indium must be diffused into the silicon wafer for depth between 0.2-0.4 llm by annealing. Practically it was found from I-V characteristics that this structure has a knee voltage at 0.8 V with very small value of reverse saturation current and 1.6 ideality factor. The maximum photo generated current of the prepared sample was about 2.3 mA at $0.396x10^{17}cm^{-3}$ of indium concentration. Theoretical & Practical results agree that the maximum photo generated current occurs at zero cell output voltage.

Paper 14

"Some Aspects of Conduction Mechanisms and Activation Energy Measurements of $Si_{1-x}Ge_x$ Thin Films" Al-Rafidain Engineering Journal, Mosul, Vol. 8(3), P. 73, (2000).

Abstract: Few samples of amorphous $Si_{1-x}Ge_x$ alloys thin films have been fabricated using Blazers (BA-105) thermal vacuum unit. Conduction mechanisms of the samples have been studied and it is proved that the current density of the sample can be calculated using the general equation of Poole - Frenkel type. It is found that there are two values of activation energy are depending on the working temperature of the films. The activation energy was as high as 0.528 eV at 450˚K while is lowered to 0.23 eV at 320˚K.Maximum variation of activation energy could be obtained at low biasing voltage and the activation energy is linearly depending on the germanium quantity in the sample. Also the activation energy could be varied as the annealing temperature is varied and minimum activation energy (around 0.12eV) is obtained at 600˚C annealing temperature.

Paper 15

"The Electrical Properties of Post-Deposition annealed and as-deposited In-Doped CdTe Thin Films" Renewable Energy Journal, England, Vol. 26(2), P.285, (2002).

Abstract: The In-doped CdTe/Si (p) heterostructure is fabricated and its electrical and photoelectrical properties are studied and interpreted. It is found that the heterojunction with Si (p+) substrate gives relatively high open circuit voltage comparing with that of Si(p) substrate. Also an electroforming phenomenon has been observed in this structure for the first time which may be considered as a memory effect.

Paper 16

"The Effect of Deposition Parameters on Hall Mobility and Carrier Concentrations" abhath al-yarmook Journal, Jordan, Vol. 11(1B), (2002).

Abstract: Many CdS thin films have been fabricated on glass substrates using vacuum thermal evaporation technique. The effect of deposition parameters on mobility and carrier concentration have been investigated using Hall measurements. It has been found that the carrier concentration and Hall mobility increased as the film thickness increased, and maximum concentration is obtained at 1.8 um thickness. An interesting relation between the carrier concentration and Hall mobility on one han and the annealing temperature on the other is noticed . Carrier concentration and Hall mobility are increased as the annealing temperature increased up to 250 ^{o}C, and then they decreased rapidly above this temperature. The fabricated films were found to be n-type. At optimized fabrication conditions (1.2um thickness 180 ^{o}C substrate temperature, 2oA/Sec deposition rate and 250 ^{o}C annealing temperature), maximum values of carrier concentration and Hall mobility are $5\times10^{16}cm^{-3}$ and $9.7cm^{2}$/V.Sec. respectively.

Paper 17

"Calculation of Light Trapping, Responsivity and Internal Quantum Efficiency of In-Doped n-Type Silicon" Renewable Energy Journal, England,

Abstract: This research is intended to investigate a mathematical model for In-doped silicon (n) structure and calculate the absorbance of the simulated cell, then study the effect of impurity photovoltaic effect on the responsivity and internal quantum efficiency using Shockley-Read-Hall model. It is found that the internal flux inside the simulated Lambertian cell could be enhanced as much as 25 times as a result of light trapping. Maximum responsivity and internal quantum efficiency of the simulated cell obtained at wavelength around 1 μm and 10^{17} cm^{-3} indium concentration. Near infrared response of the simulated cell is improved due to the enhancements of sub-band gap response by indium doping. To compare the mathematical model with the practical results few samples of In-doped n-type silicon structures have been fabricated using vacuum thermal resistive technique. Maximum responsivity and maximum internal quantum efficiency are obtained at wavelength 0.9-1 μm and 3.96×10^{17} cm-3 indium concentrations. The results of the simulated and practical cells are well agree

Paper 18

"Digital IC Testing System Based Microcontroller and FPG array", Engineering & Tech. J. Baghdad, Vol. 21(6), (2002).

Abstract: In this paper a simple low cost digital IC tester is designed and implemented. The tester performs the functional and partial DC parametric evaluation for most series of the digital integrated circuit (TTL and CMOS). The tester is based on the microcontroller AT89C51, which enables stand alone testing. The interface circuit is implemented by using the Field Programmable Gate Array (FPGA) (XC4003EPG84). Large capabilities of the FPGA made the tester hardware very flexible to realize any expansion needed in the future. The software is implemented using microcontroller machine language. The software includes a self-test and diagnosis program to test roughly the interface circuit and display existing faults. Test patterns are applied to the inputs of each IC to be tested, while the logic states of the IC pins (inputs and outputs), are read and compared to the correct (stored of simulated) words. The tester is software and hardware enable any testing algorithm to b applied to the IC for testing.

Paper 19

"The Influence of Defects on Short Circuit Current Density in p-I-n Silicon Solar Cell", Renewable Energy Journal, England, Vol.30 (2), P.187, (2005).

Abstract: The admittance analysis method has been used to calculate the collection efficiency and the short circuit current density in a-Si: H p-i-n solar cell, as a function of the thickness of i-layer. It is evident that the results of the short circuit current can be used to determine the optimal thickness of the i-layer of a cell, and it will be more accurate in comparison with the previous studies using a constant generation rate or an empirical exponential function for the generation of charge carriers throughout the i-layer.

Paper 20

”Effect of Oxide Layers and Metals on Photoelectric and Optical Properties of Schottky Barrier photo detector “, Renewable Energy Journal, England, Vol.31 (10), P…., July 2006.

Abstract: Recently a lot of attention has been paid to the Schottky barrier photo detectors due to their promising properties and easy of fabrication. Many samples of SB devices prepared by thermal deposition under high vacuum in this research. Different types and thicknesses of oxides were deposited on silicon substrate. Metals of different types and thicknesses were deposited on top of oxides. Variation of photo generated current, responsivity, quantum efficiency and detectivity as a function of incident light wavelength were measured. It was found that the shape of the curves has two maxima, one was around 500 nm and the other was around 700 nm. Ni (100)-SiO_2 –Si structure shows the maximum responsivity at 550 nm and it is equal to 400 mA/W. When comparison was made between devices of different metals; nickel layer device shows high responsivity at visible region while aluminum layer device shows high responsivity at near infrared region. Finally aluminum layer device shows detectivity higher than nickel layer device. Maximum detectivity of aluminum device was 6.4 $*10^{10}$ cm/Hz. W.

Paper 21

”Digital and Analogue storage Capability of Al/SiO_2 /Si Structures “, Asian Journal of Information technology, Vol. 5(1), P. 1-4, Jan. 2006.

Abstract: In this paper the various kinds of charge storage cells are discussed as a result of examining many samples with different structures. The C-V, I-V and R-V measurements of the structures confirm the memorization capability of MIOS devices. The examined structures reveal three kinds of memory actions. The first one is the charge storage capability which can be shown through (C-V) curve shifting as the device was exposed to certain stress for a certain time. The second is the electronic switching that is demonstrated by the fact that the switching between ON and OFF states and back to original state can only be obtained by inverting the polarity of the applied bias voltage. The third kind of memorization action is that the device can be switched into a variety of stable intermediate resistance states. The new resistance state is determined by the height of the programming pulse applied to the device. This memory action is noticed from R-V characteristic and known as a nonvolatile analogue memory behavior.

Paper 22

” Short Circuit Current Improvement of In-doped Silicon (n) Structures “, Journal of Arab Association Universities for Basic and Applied Sciences (JAAUBAS), Vol. 1(2) , P. 23, 2006.

Abstract: Theoretical and practical calculations of short circuit currents of In-doped Silicon (n) structure have been calculated. Theoretically maximum value of generated current was 5.25 mA at $0.5x10^{17}$ cm^{-3} indium concentrations. Practically the ideal I-V characteristic of the structure is obtained with indium thickness of 1500 °A annealed at 1100 °C for an hour. This structure has a knee voltage at 0.8 V with very small value of reverse saturation current and 1.6 ideality factor. The maximum photo generated current about 2.3 mA is obtained at $0.396x10^{17}$ cm^{-3} of indium concentration. Theoretical & practical results agree that the maximum photo generated current occurs at zero cell output voltage.

Paper 23

"Fast Power Loss Computation & Shunt Capacitance Insertion Using Fuzzy Logic Technique", American Journal of Applied Science. Vol.2 (2), P. 1-8, 2006.

Abstract: Fast energy loss computation is implemented using supervisory control and data acquisition system (SCADA) with personal computer. Logic Control Array (LCA) and EPROM circuits are used to implement SCADA system and to measure the active and reactive power, then draw the daily load curves for residential commercial and industrial customers. LCA, EPROM and PC are used to simplify the electronic circuits, reduce the cost and speed up the computation time. An illustrative example was done to measure, store and monitor the active power, reactive power, load voltage, load current, power factor, and the shunt capacitors current. It is found that when 2.7 MVAR bank capacitor is inserted in the network the load current is decreased from 740.8A to 688.4A and the power factor is improved from 80% up to 93%, and led to add more loads on the network and release the feeder capacitor. A rule-based fuzzy decision maker has been designed and tested with the real data collected from Jordan using SCADA system. The calculated output is almost similar to that obtained from the first approach presented in this paper. The advantage of using fuzzy decision maker is its simplicity that can be implemented on a programmable logic device and can be programmed to improve the power factor.

Paper 24

-"New Analysis to Measure the Capacitance & Conductance of MOS Structure Toward Small Size of VLSI Circuits", International Conference on Communications, Computer & P0wer (ICCCP07), Feb 19-21, 2007, Sultan Qaboos University, Oman.

Abstract: In this research thin film layers have been prepared at alternate layers of resistive and dielectric deposited on appropriate substrates to form four – terminal R-Y-NR network. If the gate of the MOS structures deposited as a strip of resistor film like NiCr, the MOS structure can be analyzed as R-Y-NR network. A method of analysis has been proposed to measure the shunt capacitance and the shunt conductance of certain MOS samples. Mat lab program has been used to compute shunt capacitance and shunt conductance at different frequencies. The results computed by this method have been compared with the results obtained by LCR meter method and showed perfect coincident with each other.